40. (New) The method of claim 39, wherein selecting comprises selecting the programming interface and wherein operating comprises programming the memory device with code using the programming interface.

41. (New) The method of claim 39, wherein selecting comprises selecting the test interface and wherein operating comprises testing the memory device for defects using the test interface.

REMARKS

Applicant respectfully requests reconsideration of this application as amended.

As a preliminary matter, in the Office Action mailed November 28, 2001, the Examiner did not attach an initialed copy of the PTO-1449 form references that were mailed to the PTO on August 10, 2001. As such, applicant respectfully requests that the Examiner indicate that these references have been considered and made of record.

Office Action Rejections Summary

Claims 19-37 have been provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-2, 4, 7-8 and 13 of copending Application No. 09293576.

Claims 19-21, 23-29, 32-35 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,031,782 of Kobashi et al. ("Kobashi").

Claims 22, 30-31 and 36-37 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Kobashi.

Status of Claims

Claims 19-41 remain pending in the application. Claims 19-21 and 24-29 and 32-35 have been amended to more properly define the invention. The amended claims are supported by the specification. Claims 38-41 have been added. No new matter has been added. No claims have been canceled.

Claim Rejections

Claims 19-37 have been provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-2, 4, 7-8 and 13 of copending Application No. 09293576.

Applicant respectfully submits that the claim numbers referred to by the Office Action do not appear to match with the claim numbers in Application no. 09293576. Nevertheless, applicant respectfully submits that the claims of the above-referenced application are not **identical** to the claims of Application no. 09293576 and, therefore, that the provisional rejection is not proper. If the Examiner believes that any of the claims from the above referenced application are **identical** to claims in Application no. 09293576, then applicant respectfully requests that the Examiner provide a side-by-side comparison of such claims.

Claims 19-21 and 23-25 have been rejected under 35 U.S.C. §102(e) as being anticipated by Kobashi. Applicant respectfully submits that amended claim 19 is not anticipated by Kobashi.

Amended claim 19 recites:

A memory device, comprising **three** different interfaces to operate the memory device in one of three different modes.

(emphasis added)

Kobashi discloses a clock buffer in a semiconductor device that includes **two** kinds of interface circuits, i.e., an LVTTL interface and an SSTL interface, that can be used to operate the device in **two** modes. By operating the device with an LVTTL interface, a current consumption can be suppressed in a self-refresh mode. In the non-refresh mode, fast transmission of signals can be performed by operating a differential amplifier which is an SSTL interface (Kobashi, col. 4, lines 21-35)(emphasis added). Nothing in Kobashi discloses a memory device having **three** different interfaces to operate the memory device in one of three different modes. Therefore, applicant respectfully submits that amended claim 19 is not anticipated by Kobashi.

Given that claims 20-21 and 23-25 depend from claim 19, applicant submits that claims 20-21 and 23-25 are also not anticipated by the cited reference.

Claims 26-29 and 32-35 have been rejected under 35 U.S.C. §102(e) as being anticipated by Kobashi. For reasons similar to those given above with respect to amended claim 19, applicant respectfully submits that claims 26-29 and 32-35 are not anticipated by the cited reference.

Claims 22, 30-31 and 36-37 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Kobashi. Applicant respectfully submits that claim 22 is patentable over Kobashi. Claim 22 depends from and includes all the limitations of amended claim 19.

Amended claim 19 recites:

> A memory device, comprising **three** different interfaces to operate the memory device in one of three different modes.

(emphasis added)

Kobashi discloses a clock buffer in a semiconductor device that includes **two** kinds of interface circuits, i.e., an LVTTL interface and an SSTL interface, that can be used to operate the device in **two** modes. By operating the device with an LVTTL interface, a current consumption can be suppressed in a self-refresh mode. In the non-refresh mode, fast transmission of signals can be performed by operating a differential amplifier which is an SSTL interface (Kobashi, col. 4, lines 21-35)(emphasis added). Nothing in Kobashi teaches or suggests a memory device having three different interfaces to operate the memory device in one of three different modes. Therefore, applicant respectfully submits that claim 22 is patentable over Kobashi.

For reasons similar to those given above with respect to claim 23, applicant respectfully submits that claims 30-31 and 36-37 are patentable over the cited reference.

Applicant respectfully submits that claim 38 is patentable over Kobashi. Claim 38 recites:

> A memory device, comprising a plurality of different interfaces to operate the memory device in a plurality of different modes, wherein the memory device is a flash memory and wherein one of the plurality of interfaces is **a standard flash memory interface**.

(emphasis added).

Kobashi discloses a clock buffer in a semiconductor device that includes two kinds of interface circuits, i.e., an LVTTL interface and an SSTL interface, that can be used to operate the device in two modes. By operating the device

with an LVTTL interface, a current consumption can be suppressed in a self-refresh mode. In the non-refresh mode, fast transmission of signals can be performed by operating a differential amplifier which is an SSTL interface (Kobashi, col. 4, lines 21-35)(emphasis added). Nothing in Kobashi teaches or suggests a flash memory device having a plurality of interfaces wherein one of the interfaces is a standard flash memory interface, as recited in claim 38. Therefore, applicant respectfully submits that claim 38 is patentable over Kobashi.

Applicant respectfully submits that claim 39 is patentable over Kobashi. Claim 39 recites:

> A method, comprising:
> selecting an interface from among at least a **programming** interface and a **test** interface in a memory device; and
> operating the memory device with the selected interface.

(emphasis added).

Kobashi discloses a clock buffer in a semiconductor device that includes two kinds of interface circuits, i.e., an LVTTL interface and an SSTL interface, that can be used to operate the device in two modes. By operating the device with an LVTTL interface, a current consumption can be suppressed in a self-refresh mode. In the non-refresh mode, fast transmission of signals can be performed by operating a differential amplifier which is an SSTL interface (Kobashi, col. 4, lines 21-35)(emphasis added). As such, both interfaces are used with operation modes of the device.

In contrast, claim 39 recites selecting an interface from among at least a programming interface and a test interface in a memory device. Nothing in Kobashi teaches or suggest a programming interface or a test interface.

Therefore, applicant respectfully submits that claim 29 39 is patentable over Kobashi.

Given that claims 40-41 depend from claim 39, applicant submits that claims 40-41 are also patentable over Kobashi.

In conclusion, applicants respectfully submit that in view of the amendments and arguments set forth herein, the applicable rejections have been overcome and the claims are in condition for allowance.

If there are any additional charges, please charge our Deposit Account No. 02-2666.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

MARKED-UP VERSION OF THE AMENDED CLAIMS

A marked up version of the amended claims ___ is provided below. Additions are indicated with "__" and deletions are indicated within "[ ]."

19. (Amended) A memory device, comprising [a plurality of] three different interfaces to operate the memory device in [a plurality of] one of three different modes.

20. (Amended) The memory device of claim [19] 21, further comprising [a configuration device] selection circuitry to select among the plurality of different interfaces.

21. (Amended) The memory device of claim [20] 19, wherein the [plurality of] three different interfaces comprise[s]:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

24. (Amended) The memory device of claim 20, wherein the [configuration device] selection circuitry comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

25. (Amended) The memory device of claim 24, wherein the [plurality of] three different interfaces comprises:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

26. (Amended) A component board, comprising:

a processor; and

a memory device coupled with the processor, the memory device comprising [a plurality of] three different interfaces to operate the memory device in [a plurality of] one of three different modes.

27. (Amended) The component board of claim 26, further comprising [a configuration device] selection circuitry to select among the [plurality of] three different interfaces.

28. (Amended) The component board of claim 27, wherein the [configuration device] selection circuitry comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

29. (Amended) The component board of claim [28] 26, wherein the [plurality of] three different interfaces comprise[s]:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

32. (Amended) A computer system, comprising:

a peripheral device; and

a system board coupled to the peripheral device, the system board comprising:

a processor; and

a memory device coupled with the processor, the memory device comprising [a plurality of] three different interfaces to operate the memory device in [a plurality of] one of three different modes.

33. (Amended) The computer system of claim 32, further comprising [a configuration device] selection circuitry to select among the [plurality of] three different interfaces.

34. (Amended) The computer system of claim 33, wherein the [configuration device] selection circuitry comprises:

a plurality of drivers, each of the plurality of drivers coupled between a device pad and a device circuit, each of the plurality of drivers having a control input; and

a multiplexer coupled to the control input of each of the plurality of drivers to select one of the plurality of drivers.

35. (Amended) The computer system of claim [34] 32, wherein the [plurality of] three different interfaces comprise[s]:

a test interface to test the memory device for defects;

a programming interface to program the memory device with a code; and

an operation interface to operate the memory device in an operation mode.

Claims 38-41 have been added.